UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,844	06/01/2004	Graham Balsdon	021648-000700US	3843

51111 7590 03/22/2007

AKA CHAN LLP
900 LAFAYETTE STREET
SUITE 710
SANTA CLARA, CA 95050

EXAMINER	
LEVIN, NAUM B	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,844	BALSDON ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-14 and 21-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-14 and 21-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/709,844, and Amendment filed on 01/03/2007. Independent claims 1, 9 and 13 have been amended by including additional limitation. Claims 21-30 have been newly added. Claims 6 and 15-20 have been cancelled. Claims 1-5, 7-14 and 21-30 remain pending in the application.

2. By amending claim 1, which necessitates a changing the ground for rejection, and the fact that claims 2-5 and 7-8 are dependent from claim 1, the new rejection of claims 1-5 and 7-8 was necessitated by applicants' amendment.

By amending claim 9, which necessitates a changing the ground for rejection, and the fact that claims 10-12 are dependent from claim 9, the new rejection of claims 1 9-12 was necessitated by applicants' amendment.

By amending claim 13, which necessitates a changing the ground for rejection, and the fact that claim 14 is dependent from claim 13, the new rejection of claims 13-14 was necessitated by applicants' amendment.

Claim Objections

3. Claims 2-5 and 8 recite the limitation "the automatic router tool". There is insufficient antecedent basis for this limitation in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 5-11, 13-16 and 18-20 are rejected under 35 U.S.C. 102(e) as being unpatentable by Lin (US Pub. No.: 20060080630).

5. As to claims 1, 9 and 13 Lin discloses:

(1) An electronic automation system comprising:

a database of an integrated circuit design (The floor plan design data may be created or stored in any conventional data format that will represent the desired floor plan design structures ... such as ... the "Open Access" database format – [0038]);

a mouse input device (The input devices 123 may include ... a pointing device such as a mouse ...- [0032], Fig.1);

a graphical user interface tool, capable of accessing and performing operations on the database, based on input from the mouse input device (the floor planning tool 201 allows a designer to easily position components of a microcircuit in a floor plan design, while maintaining desired attributes for the design. ... By using a pointing device, such as a keyboard, mouse, stylus, touchpad, joystick or the like, a circuit designer can select and move the placement of one or more of the blocks making up the floor plan design. As the designer moves a selected "target" block, the user interface graphically displays the various changes in the circuit characteristics and design that will result from the movement of the target block - [0027], Fig.2) ([0027]; [0039]); and

a shape-based automatic router tool, capable of accessing the database, to create a interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse (floor plan design tool 201, the circuit layout determination module 207 may employ a multi-step algorithm to automatically determine the routing of a wire network, such as a power/ground wire network. This algorithm may include, for example, (1) the construction of a visibility graph corresponding to the current arrangement of the floor plan design, (2) wire segment insertion into the design, (3) initial construction of the wire routing, and, (4) refinement of the wire routing - [0108], Fig.2), wherein the interconnect route path comprises segments having different interconnect widths (... if a channel box corresponds to a horizontal primary edge in the visibility graph, then a vertical wire segment is inserted into the channel box. Similarly, a horizontal wire segment for each needed power and ground network is inserted into each channel box corresponding to a vertical primary edge in the visibility graph. As discussed in detail above, the width of the inserted wire segment is calculated based upon the applicable attributes for that channel box - [0111]) using **flood operations** (If a wire's or via's determined current density value exceeds its specified maximum allowable current density value, then the PG wiring analysis module 1007 increases the width of the wire or via to correct this electromigration problem in step 1307- [0128]) ([0026]; [0027]; [0030]; [0035]; [0080]-[0083]; [0093]; [0094]; [0108]; [0111]; [0117]; [0128]);

(9) A method of designing an integrated circuit comprising:

using at least one flooding operation ((If a wire's or via's determined current density value exceeds its specified maximum allowable current density value, then the PG wiring analysis module 1007 increases the width of the wire or via to correct this electromigration problem in step 1307- [0128]) to determine an interconnect route path between a first point and a second point of an integrated circuit design (a path between two blocks in the floor plan design is defined as an edge in the data structure describing the complete visibility graph ... empty space serves as a channel area or channel "box" through which connection wires, such as power/ground network wires, can be routed - [0072]; [0128]);

comparing a property of the interconnect route path to a design rule (The PG wiring analysis module 1007 then compares the determined current density for each wire and via with the maximum current density allowable for the wire or via in step 1305 ... This maximum current density value allowable for each wire and via may be specified, for example, by the foundry that will be manufacturing integrated circuits from the design - [0127]);

if the property of the first interconnect path violates the design rule, creating an interconnect line for the interconnect route path having a first width (If a wire's or via's determined current density value exceeds its specified maximum allowable current density value, then the PG wiring analysis module 1007 increases the width of the wire or via to correct this electromigration problem in step 1307 - [0128]) ([0128]- [0131]; [0134]- [0137]); and

if the property of the first interconnect path meets the design rule, creating the interconnect line for the interconnect route path having a second width, different from the first width (Once the identified wiring problems in the received floor plan design 1201 have been corrected, or if the PG wiring analysis module 1007 determines that there are no wiring problems in the received floor plan design 1201, then the floor plan design 1201 is provided to the area minimization module 1003. ... and then employs the well-known "Simplex" algorithm to determine the minimum suitable dimensions for each wire segment in the wiring of the received floor plan design 1201 - [0140]);

(13) A method of designing an integrated circuit comprising:

using at least one flooding operation ((If a wire's or via's determined current density value exceeds its specified maximum allowable current density value, then the PG wiring analysis module 1007 increases the width of the wire or via to correct this electromigration problem in step 1307- [0128]) to determiner an interconnect route path between a first point and a second point of an integrated (a path between two blocks in the floor plan design is defined as an edge in the data structure describing the complete visibility graph ... empty space serves as a channel area or channel "box" through which connection wires, such as power/ground network wires, can be routed - [0072]; [0128]);

determining a property of the interconnect route path [0127]); and

creating an interconnect line for the interconnect route path having a width based on the property of the interconnect route path and a design rule ([0128]- [0131]; [00134]-[00137]).

7. As to claims 5, 7-8, 10-11 and 14 Lin recites:

(5) The system, wherein the automatic router tool uses at least one of Steiner tree algorithm ([0133]);

(7) The system, wherein the integrated circuit design comprises at least one of a, digital, analog integrated circuit ([0103]- [0106]);

(8) The system, wherein automatic router tools create interconnect route paths for two or more nets ([0111]);

(10), (11), (14) The method, wherein the property is a current requirement of the interconnect route path ([0006]; [0127]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable by Lin in view of Balakrishnan et al. ("A greedy router with technology targetable output"; 4-6 March 1999 Page(s): 252 - 255).

As to claim 23 Lin recites:

(23) An electronic automation system comprising:

a database of an integrated circuit design (The floor plan design data may be created or stored in any conventional data format that will represent the desired floor plan design structures ... such as ... the "Open Access" database format – [0038]);

a mouse input device (The input devices 123 may include ... a pointing device such as a mouse ...- [0032], Fig.1);

a graphical user interface tool, capable of accessing and performing operations on the database, based on input from the mouse input device (the floor planning tool 201 allows a designer to easily position components of a microcircuit in a floor plan design, while maintaining desired attributes for the design. ... By using a pointing device, such as a keyboard, mouse, stylus, touchpad, joystick or the like, a circuit designer can select and move the placement of one or more of the blocks making up the floor plan design. As the designer moves a selected "target" block, the user interface graphically displays the various changes in the circuit characteristics and design that will result from the movement of the target block - [0027], Fig.2) ([0027]; [0039]); and

a shape-based automatic router tool, capable of accessing the database, to create a interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse (floor plan design tool 201, the circuit layout determination module 207 may employ a multi-step algorithm to automatically determine the routing of a wire network, such as a power/ground wire network. This algorithm may include, for example, (1) the construction of a visibility graph corresponding to the current arrangement of the floor plan design, (2) wire

segment insertion into the design, (3) initial construction of the wire routing, and, (4) refinement of the wire routing - [0108], Fig.2), wherein the interconnect route path comprises segments having different interconnect widths (... if a channel box corresponds to a horizontal primary edge in the visibility graph, then a vertical wire segment is inserted into the channel box. Similarly, a horizontal wire segment for each needed power and ground network is inserted into each channel box corresponding to a vertical primary edge in the visibility graph. As discussed in detail above, the width of the inserted wire segment is calculated based upon the applicable attributes for that channel box - [0111]) using **flood operations** (If a wire's or via's determined current density value exceeds its specified maximum allowable current density value, then the PG wiring analysis module 1007 increases the width of the wire or via to correct this electromigration problem in step 1307- [0128]) ([0026]; [0027]; [0030]; [0035]; [0080]-[0083]; [0093]; [0094]; [0108]; [0111]; [0117]; [0128]).

With respect to claim 23 Lin teaches the features above but lacks an electronic design automation system that uses a greedy algorithm to create an interconnect route path.

As to claim 23 Balakrishnan discloses:

an electronic design automation system that uses a greedy algorithm to create an interconnect route path (Our objective was to integrate an effective channel routing algorithm with the Chip Design Language (CDL) algorithmic layout tool. CDL uses technology targetable layout techniques, so that the output of the routing algorithm can easily be ported to different technologies. We introduce the technology independent

features of CDL and describe how a greedy router can be interfaced to it. - Abstract) (Abstract; pp.1-2).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Balakrishnan's teaching regarding the electronic design automation system that uses a greedy algorithm to create an interconnect route path and use it in Lin's invention to improve electronic design by making it more technology targetable.

9. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable by Lin in view of Hathaway et al. (US Patent 5,737,580).

As to claims 24-25 Lin recites:

(24), (25) An electronic automation system comprising:

a database of an integrated circuit design (The floor plan design data may be created or stored in any conventional data format that will represent the desired floor plan design structures ... such as ... the "Open Access" database format – [0038]);

a mouse input device (The input devices 123 may include ... a pointing device such as a mouse ...- [0032], Fig.1);

a graphical user interface tool, capable of accessing and performing operations on the database, based on input from the mouse input device (the floor planning tool 201 allows a designer to easily position components of a microcircuit in a floor plan design, while maintaining desired attributes for the design. ... By using a pointing device, such as a keyboard, mouse, stylus, touchpad, joystick or the like, a circuit designer can select and move the placement of one or more of the blocks making up

the floor plan design. As the designer moves a selected "target" block, the user interface graphically displays the various changes in the circuit characteristics and design that will result from the movement of the target block - [0027], Fig.2) ([0027]; [0039]); and

a shape-based automatic router tool, capable of accessing the database, to create a interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse (floor plan design tool 201, the circuit layout determination module 207 may employ a multi-step algorithm to automatically determine the routing of a wire network, such as a power/ground wire network. This algorithm may include, for example, (1) the construction of a visibility graph corresponding to the current arrangement of the floor plan design, (2) wire segment insertion into the design, (3) initial construction of the wire routing, and, (4) refinement of the wire routing - [0108], Fig.2), wherein the interconnect route path comprises segments having different interconnect widths (... if a channel box corresponds to a horizontal primary edge in the visibility graph, then a vertical wire segment is inserted into the channel box. Similarly, a horizontal wire segment for each needed power and ground network is inserted into each channel box corresponding to a vertical primary edge in the visibility graph. As discussed in detail above, the width of the inserted wire segment is calculated based upon the applicable attributes for that channel box - [0111]) using **flood operations** (If a wire's or via's determined current density value exceeds its specified maximum allowable current density value, then the PG wiring analysis module 1007 increases the width of the wire or via to correct this

electromigration problem in step 1307- [0128]) ([0026]; [0027]; [0030]; [0035]; [0080]-[0083]; [0093]; [0094]; [0108]; [0111]; [0117]; [0128]).

With respect to claims 24-25 Lin teaches the features above but lacks an electronic automation system further comprising file accessible by the shape-based automatic router tool, comprising data describing current density as a function of net frequency.

As to claim 24-25 Hathaway teaches:

an electronic automation system (A technique to optimize the width of automatically routed wire segments - Abstract) further comprising file accessible by the shape-based automatic router tool (The known values for these variables are input from the circuit library, which is accessible by each of the tools described herein at any point – col.5, ll.50-52), comprising data describing current density as a function of net frequency (The following equation can be used to define a maximum downstream capacitance: C.sub.ds =[I.sub.max.times.S.times.T.times.L]/ [2.times.F.times.V] where ... F is the frequency of operation in Hertz input to each net to be checked – col.5, ll.37-49 ... The capacitive effects are dependent upon the layout of the various IC components. Thus, a better designed layout can also contribute to a reduction in capacitive effects which, in turn, reduces current density – col.2, ll.2-6) (Abstract; col.1, ll.58-67; col.2, ll.1-6; col.5, ll.37-52).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Hathaway's teaching regarding the electronic automation system further comprising file accessible by the shape-based automatic router tool,

comprising data describing current density as a function of net frequency and use it in Lin's invention to improve an efficiency of the electronic automation system by using relationship between current density and frequency, thereby performing more accurate and reliable predictor of electromigration risk for high speed integrate circuits.

10. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable by Lin in view of Tripathi et al. (US Patent 6,109,775).

As to claim 30 Lin recites:

(30) A method of designing an integrated circuit comprising:

automatically determining an interconnect route path between a first point and a second point of an integrated circuit design (a path between two blocks in the floor plan design is defined as an edge in the data structure describing the complete visibility graph ... empty space serves as a channel area or channel "box" through which connection wires, such as power/ground network wires, can be routed - [0072]; [0128]);

determining a property of the interconnect route path (In step 1303, the PG wiring analysis module 1007 determines the `current density` values of each wire and via – [0127]); and

creating an interconnect line for the interconnect route path having a width based on the property of the interconnect route path (If a wire's or via's determined current density value exceeds its specified maximum allowable current density value, then the PG wiring analysis module 1007 increases the width of the wire or via to correct this electromigration problem in step 1307 – [0128]) .

With respect to claim 30 Lin teaches the features above but lacks a method of designing an integrated circuit further comprising creating an interconnect line having a width based on optical proximity effects.

As to claim 30 Tripathi discloses:

a method of designing an integrated circuit comprising creating an interconnect line having a width based on optical proximity effects (The formation of a grid superimposed on the surface of an integrated circuit structure has been used ... to correct for optical proximity problems ... resulting in either a widening or narrowing of the equivalent metal lines – col.13, ll.52-59) (col.4, ll.42-46; col.4, ll.66-67; col.13, ll.52-67; col.14, ll.1-11).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Tripathi teaching regarding the method of designing an integrated circuit (IC) further comprising creating an interconnect line having a width based on optical proximity effects and use in Lin's invention to improve an efficiency of the integrated circuit design by increasing precision and reliability of IC design.

11. As to claim 2-4, 26-27 Hathaway recites:

An electronic automation system (A technique to optimize the width of automatically routed wire segments - Abstract) further comprising file accessible by the shape-based automatic router tool (The known values for these variables are input from the circuit library, which is accessible by each of the tools described herein at any point – col.5, ll.50-52), comprising data describing current density as a function of net frequency (The following equation can be used to define a maximum downstream

capacitance: C.sub.ds =[I.sub.max.times.S.times.T.times.L]/ [2.times.F.times.V] where ... F is the frequency of operation in Hertz input to each net to be checked – col.5, ll.37-49 ... The capacitive effects are dependent upon the layout of the various IC components. Thus, a better designed layout can also contribute to a reduction in capacitive effects which, in turn, reduces current density – col.2, ll.2-6), wherein when frequency is not provided for a net DC operation will be assumed (... S is an AC current adjust constant based on chip technology – col.5, ll.42-43) (Abstract; col.1, ll.58-67; col.2, ll.1-6; col.5, ll.37-52).

12. As to claim 12 Tripathi discloses:

(12) The method, wherein the design rule is an optical proximity effect correction rule (col.4, ll.42-46; col.4, ll.66-67; col.13, ll.52-67; col.14, ll.1-11).

13. As to claims 21, 22 Lin recites:

(21) The system, wherein automatic router tool creates a first, a second, a third net (routing of data signal, control signal, power and ground wires – [0007]) having different width (the circuit attributes storage module 209 may include attributes relating to the routing of the wires making up the power and ground networks. These attributes may, for example, dictate the width of the main power and ground wires – [0076]) ([0007]; [0076]);

(22) The system, wherein automatic router tool performs detailed routing (There are two types of routing for electrical connection wires: global routing and detailed (or "local") routing – [0008].

14. As to claims Lin recites:

As to claims 28, 29 Balakrishnan discloses:

an electronic design automation system that uses a greedy algorithm to create an interconnect route path (Our objective was to integrate an effective channel routing algorithm with the Chip Design Language (CDL) algorithmic layout tool. CDL uses technology targetable layout techniques, so that the output of the routing algorithm can easily be ported to different technologies. We introduce the technology independent features of CDL and describe how a greedy router can be interfaced to it. - Abstract) (Abstract; pp.1-2).

15. Examiner finds Applicant's arguments as none persuasive, because as indicated above the references read on the claims as presently written. However, Applicants' arguments are to look are well taken.

16. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N L

VUTHE SIEK
PRIMARY EXAMINER